# Ferroelectric Hafnium Dioxide Thin Films

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***Abstract*—Ferroelectric memory shows great promise as a high speed alternative to conventional memory architectures. Traditionally this memory has been constrained to niche applications due to the large size of ceramic-based ferroelectric devices. Doped hafnium dioxide measured on a newly-acquired aixACCT TF Analyzer 1000 is shown to have ferroelectricity an order of magnitude stronger than discrete PZT films that were measured, enabling further scaling while also simplifying fabrication via the elimination of ceramics from the process flow. Additionally, the presence of a TiN capping layer as well as a lower temperature, long duration anneal are shown to be key in obtaining a potential ferroelectric phase in hafnium dioxide.**

***Index Terms*—Ferroelectricity, Hafnium Dioxide, FeFET.**

## I. Introduction

FOR fifty years now, the semiconductor industry has been driven by Moores law an observed trend turned into a benchmark standard that states that the number of transistors on an integrated circuit (IC) doubles every 18 months. With this trend has come aggressive scaling of device sizes to enable greater packing density and efficiency. This has been enabled by constant innovation in lithography for patterning as well as in transistor architecture and materials to prevent degradation of device electrical performance.

Despite these advances, there is a fundamental limit to how small devices can be made. As devices reach smaller and smaller nodes they draw closer and closer to the atomic radii of the atoms that make up the films in a transistor. Once these limits are reached, scaling as it is known currently will come to an end. Even current memory devices are reaching the point where there are a countable number of stored charges that are the difference between a stored one and a stored zero. For this reason, non-charge memories are an active area of research, with several being highlighted by the International Technology Roadmap for Semiconductors (ITRS) [1]. One such category of non-charge based memories are those based on ferroelectricity.

## II. Theory

Ferroelectricity is a phenomenon exhibited whereby materials exhibit charge generation when electrical fields are applied. These materials are a subset of pyroelectric materials (charge generation by thermal fields), which are themselves a subset of piezoelectric materials (charge generation via mechanical fields). This hierarchy is shown in Figure 1. Practically, this effect is seen as the presence of two stable atomic locations, known as polarization states, in a ferroelectric crystal lattice. The atoms will move between these locations or polarizations based on the applied electric field.

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Ferroelectric behavior can be quantified through a hysteresis loop, obtained via a polarization vs. voltage measurement. Such a loop is seen in Figure 2. Once polarized for the first time, a ferroelectric device will ideally either be in the up or down polarization and would rest at one of the relaxed remnant polarizations (labeled $P_r$ in the Figure). If the material lays at $P_r$- and a positive bias is applied, the ferroelectric domains begin to change polarization and a rapid increase in polarization is seen until the domains have all changed polarization. At this point, the curve levels out again and increases only linearly with increasing bias. Once the bias is removed, the material relaxes to $P_r$+.

Another parameter of note is the coercive voltage the voltage at which the material passes through zero polarization during switching. The coercive field for a ferroelectric material can be found by dividing this voltage by the thickness of the material. This is a good measure of the ferroelectric strength of the sample as a material with a higher coercive field with require less thickness to get the same 2*$V_c$ window. For an excellent primer on further theory behind P-V measurements, the reader is referred to Radiant Technologies Inc.s publication on ferroelectric characterization. [2]

In hafnium dioxide, $HfO_2$, ferroelectricity is believed to be caused by a non-centrosymmetric orthorhombic phase (Pbc21). While this crystal phase was not seen previously in $HfO_2$, its presence in $ZrO_2$ and the similarity between $HfO_2$ and $ZrO_2$ make such an argument plausible. This hypothesis is also supported by XRD data. This ferroelectric phase is illustrated in Figure 3. The transition to this phase is made more favorable via the presence of a capping layer as well as the doping of the $HfO_2$. [3] Since this ferroelectric phases discovery, several dopants including Si, Al, and Y have been shown to induce ferroelectricity in $HfO_2$ at varying concentrations. [4]

One form of memory based on ferroelectric materials is the ferroelectric field effect transistor (FeFET). This transistor is being eyed as a potential future memory solution based on its small cell size (1T) and fast operation (sub-100 ns). There are also hopes that this architecture could be used as a nonvolatile memory solution if data retention time is improved. [5] A diagram of one type of FeFET can be seen in Figure 4.

$HfO_2$ shows great promise as a FeFET ferroelectric layer when compared to the ceramic materials traditionally used in ferroelectric devices. Historically, lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT) based ferroelectric memory devices have been constrained to niche markets due to their low overall capacities. This is due to a variety of factors that make the idea of scaling these devices untenable. First off, these ceramic materials suffer from poor compatibility with standard complementary metal-oxide-semiconductor (CMOS) fabrication flows. These devices require a thick buffer layer to

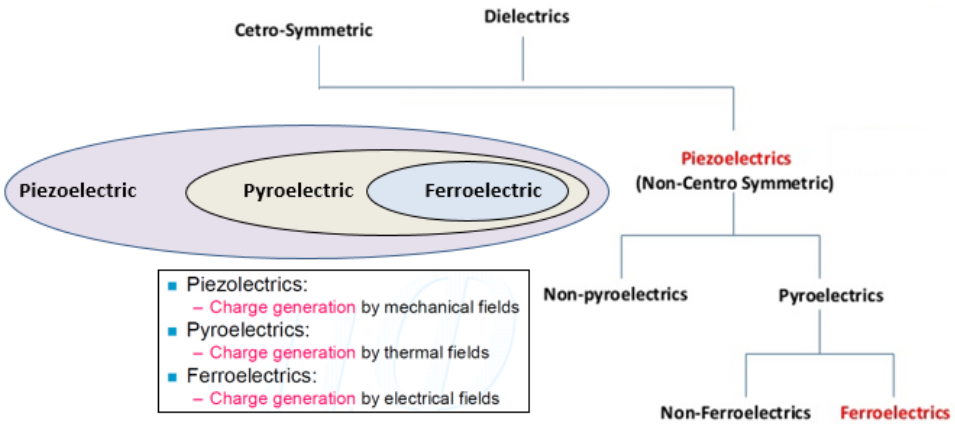


Fig. 1. Hierarchy of dielectric materials pertaining to ferroelectricity.

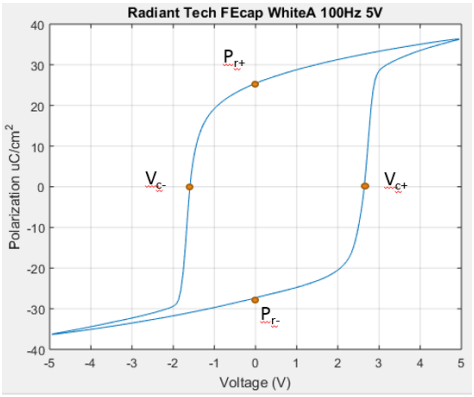


Fig. 2. Typical hysteresis of a ferroelectric film (material travels along loop in anticlockwise direction).

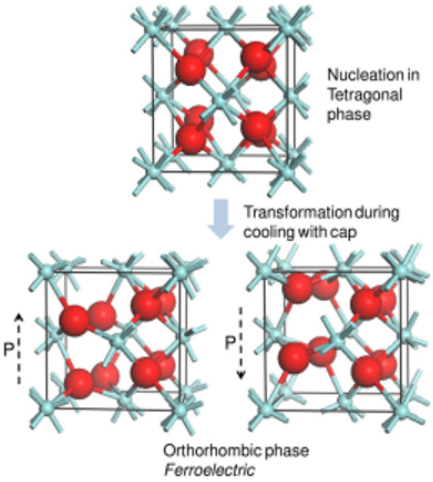


Fig. 3. Visualization of orthorhombic phase in $HfO_2$. [3]

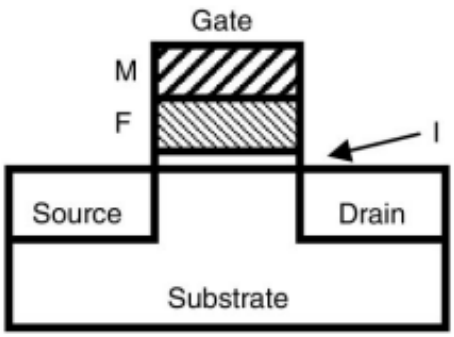


Fig. 4. Basic MFIS FeFET structure. [6]

allow for good interfacial properties and prevent intermixing of the perovskite with the silicon channel. [1] This buffer layer, by increasing the thickness of the gate stack, limits the scalability the device. As the gate stack aspect ratio increases there are a variety of physical processing concerns that come into play.

Beyond the physical stability concerns of the gate stack, this thick buffer layer also greatly hurts electrical performance. As the buffer layer is a dielectric material, there exists a series combination of a ferroelectric and finite dielectric capacitor. When this is the case, charge balance at the node between the devices will lead to the presence of an electric field across the ferroelectric capacitance that acts to depolarize the capacitor, returning the system to equilibrium. [6] This limits the data retention time of traditional ferroelectric transistors, thus preventing their widespread use as an alternative for nonvolatile solid state memory.

$HfO_2$, on the other hand, is widely understood and already in use as a high-k gate dielectric. It does not require a thick buffer layer, increasing the dielectric series capacitance and limiting the depolarization field. This increases theoretical retention time. Beyond this, $HfO_2$ also exhibits a much stronger coercive field than perovskite materials on the order of 1 MV/cm versus 50 kV/cm or so. [5] The difference this makes in the gate stack aspect ratio is highlighted in Figure 5. Most $HfO_2$ films, including most of those in studies

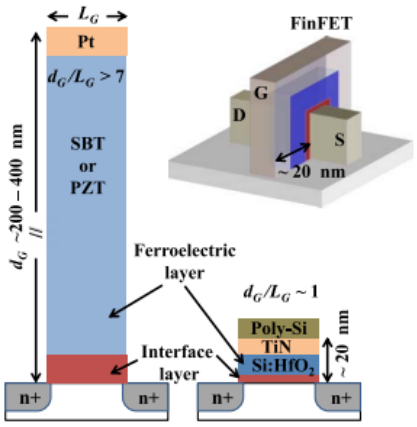


Fig. 5. $textrmHfO_2$-based Ferroelectric device shows significant reduction in gate stack height and potential for use in finFET applications. [5]

of the ferroelectric phase, have been deposited via atomic layer deposition (ALD). Notably, however, ferroelectricity has also been observed in co-sputtered yttrium doped $HfO_2$ films (Y:$HfO_2$, albeit at lower doping levels. [3], [4], [7]–[9] This observation is what forms the basis for the work hereafter discussed in this paper.

## III. Experimental Details

In order to enable ferroelectric research at RIT, several process flows were design to investigate novel methods for doping sputtered $HfO_2$ films. Sputtered films were investigated in an effort to allow the entire device process flow to be completed in the RIT Semiconductor and Microsystems Fabrication Laboratory (SMFL) as they have no ALD capabilities. Deposition was done in a CVC 601 DC magnetron sputter tool with reactive sputter of a hafnium target and non-reactive sputter of an aluminum target. All Hf and Al sputters were done at 100 W. $HfO_2$ was sputtered with a 6 mT partial pressure of Ar and 0.75 mT of $O_2$. Flow rates for Ar and $O_2$ were 29 sccm and 5.6 sccm respectively. Al sputtering was done by simply turning off $O_2$ flow and sputtering at 6 mT Ar. This tool was also used to deposit TiN via reactive sputter of a titanium target. TiN sputters were done at 110 W for 1154 s. Gas flows for the TiN sputter were 23 sccm (4.8 mT) for Ar and 16 sccm (1.2 mT) for $N_2$. Lift-off was used for patterning to avoid concerns with etching these films.

The first general approach tried was to sputter a hafnium oxide stack with several thin Al layers interspersed through its thickness. This was done to attempt to obtain uniform Al doping throughout the $HfO_2$. This process flow can be seen in Figure 6. The TiN layer is sputtered on after the $HfO_2$ and liftoff performed before the capacitors are annealed. Lithography is then performed again and Al is evaporated on the front and back to finish the devices.

The second approach taken was to deposit a thicker Al layer on top of a solid $HfO_2$ layer and attempt to drive in the Al much like would be done with a solid source dopant. An experiment was performed with this method investigating the importance of four different factors on obtaining a ferroelectric phase. These included a TiN capping layer above the Al:$HfO_2$, a TiN layer before the Al:$HfO_2$, the method and temperature of anneal (1 hr 600 °C furnace, 20 s 850 °C RTA, or 1s 1000 °C RTA), and method of Al dopant deposition (evaporation vs sputtering). These are all highlighted, along with the process flow, in Figure 7.

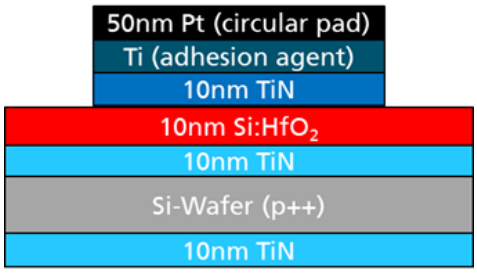


Fig. 8. Doped $HfO_2$ capacitor structure (provided courtesy of NaMLab)

TABLE I
Layer thicknesses in nm of deposited films

| Layer | Sandwich Doped | Solid Source Doped |
|---|---|---|
| TiN | 14.8 | 15.0 |
| $HfO_2$ | 16.6 | 15.5 |

Upon completion, devices were tested with an MDC C-V probing station (hot chuck at 27 °C, HP 4284A LCR Meter). Attempts were also made to test the devices with a brand new Advanced Customized Characterization Technologies TF Analyzer 1000 (TF 1000) ferroelectric test instrument. This instrument was validated on discrete samples and also used to test some ferroelectric and antiferroelectric Si:$HfO_2$ samples obtained from NaMLab, the group that discovered ferroelectric behavior in doped $HfO_2$. The structure of these capacitors is shown in Figure 8.

## IV. Results and Discussion

### A. Process Results

During processing, monitor wafers were included with every deposition step to allow for easy measurement. Thicknesses of these films were measured using variable angle spectroscopic ellipsometry (VASE) measurements. These measurements are summarized in Table 1.

Unfortunately, several samples using the sandwich Al doping approach exhibited physical film failure during anneal. This is highlighted in Figure 9, where the buckling up of a film can be seen. Notably, this buckling only occurs around the capacitors where there is no TiN cap. This indicates that the buckling itself must be coming from the Al:$HfO_2$ stack. As this problem was not seen in undoped $HfO_2$ capacitors, it is believed that the multi-layered approach taken is the culprit. The additional films in the stack provide additional stress whereas the additional interfaces provide additional points for failure. For this reason, it is recommended that this process not be used unless an extensive study can be done on film stresses and the process window that would yield a stable film. As this is likely to be a complicated endeavor, it was decided to focus on the solid source doping approach for a more detailed study.

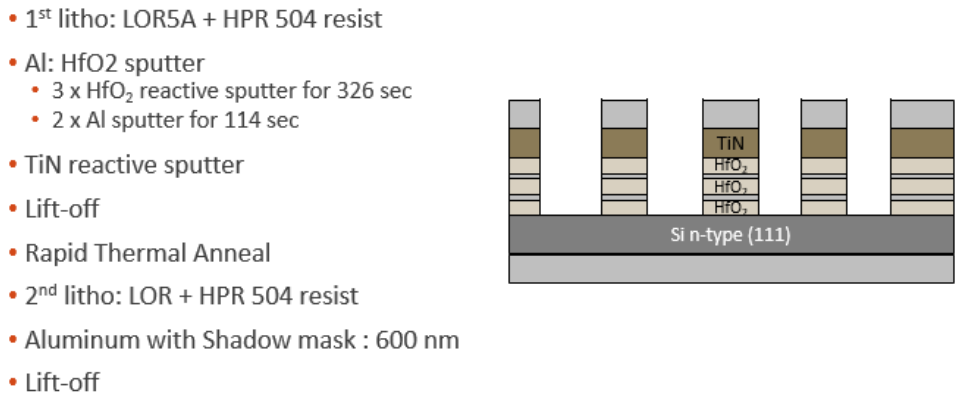


Fig. 6. Al/$HfO_2$ sandwich-doping approach. Light grey layers indicate Al.

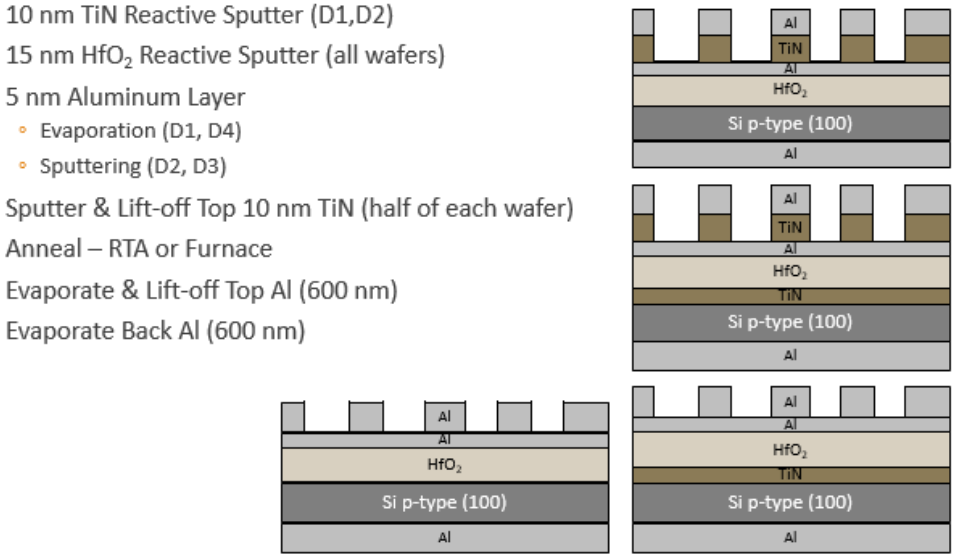


Fig. 7. Devices fabricated with the solid-source dopant approach. Top and bottom Al layers not to scale.

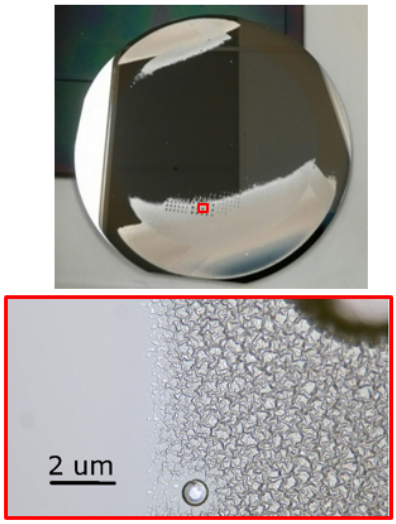


Fig. 9. Wafer exhibiting film failure at top and bottom due to compressive stress, seen in the micrograph.

On the whole, processing of the solid source doping samples went more smoothly. No failure of the films upon anneal was observed and most of the samples made it to electrical test. The one exception was those samples with a sputtered Al dopant layer. This Al layer developed away during 1st level lithography. This may be an indicator that the sputtered film is more porous than the evaporated film, perhaps because of the low power used to sputter the Al. If the atoms did not have sufficient energy to coalesce they will have simply hit the wafer and adsorbed, leading to a low quality film. Evaporated Al, on the other hand, has plenty of thermal energy and the atoms can move around to form a dense film.

### *B. Electrical Results*

Of the solid source dopant samples that made it to electrical test, promising results were seen in those samples with a TiN capping layer above the $HfO_2$ that were annealed at the lower two temperatures. The C-V curves for these samples are highlighted in Figure 10. The fact that these windows in the C-V curve are not dependent on different sweep speeds

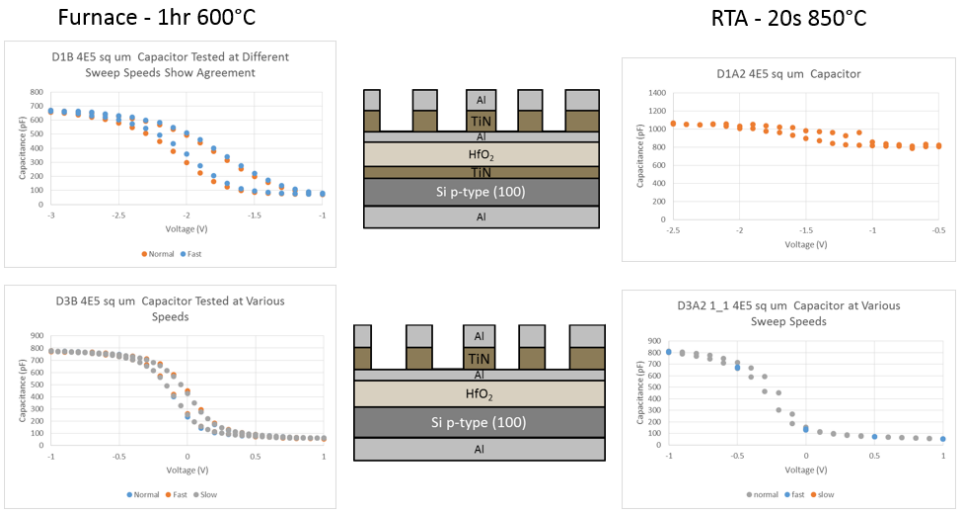


Fig. 10. Promising C-V results seen in samples with TiN cap.

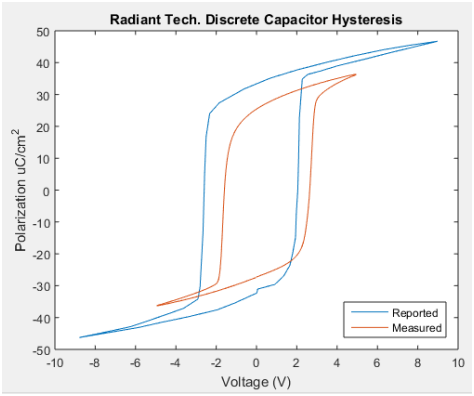


Fig. 11. Ferroelectric PZT reference capacitor hysteresis shows relatively good agreement with reported data. [10]

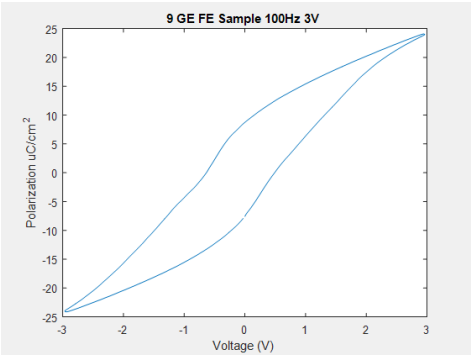


Fig. 12. Ferroelectric Si:$HfO_2$ exhibits 0.75 V coercive voltage and 10 uC/cm$^2$ $P_r$

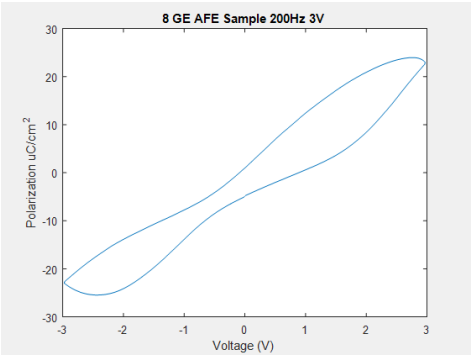


Fig. 13. Antiferroelectric $HfO_2$ sample, showing how ferroelectricity can be modulated based on doping level.

shows that the behavior may be caused by hysteresis rather than mobile charges.

When obtained, the first thing done with the TF 1000 was to validate correct setup by measuring ferroelectric capacitors of known size and comparing data to that reported. This was done with discrete ferroelectric lead zirconate titanate (PZT) capacitors obtained from Radiant Technologies, Inc. The comparison of RIT measured data with company reported typical performance data can be seen in Figure 11. Given that this data lined up relatively well, the tool was next used to measure the Si-doped $HfO_2$ samples provided by NaMLab. These results can be seen in Figures 12 and 13 for the ferroelectric and antiferroelectric samples and line up well with values reported in literature produced by the group. [4], [7] Notably, the 10 nm $HfO_2$ film exhibits a coercive field 10x greater than that of the PZT-based Radiant Technologies capacitor.

Efforts were made to measure these devices on the TF 1000 tester however the depletion capacitance of the MIS structure masked any potential ferroelectric effects. For this reason, MIM capacitors were fabricated using the same process flow on a degenerately doped substrate. C-V testing of these samples yielded a dielectric constant for the $HfO_2$ around 16 rather than the value of 3-4 seen in the MIS samples previously created. These samples yielded no measurable hysteresis but that is not surprising as they are in a non-ferroelectric high-k phase. For comparison, the NaMLab samples yielded a dielectric constant of 4.2 when measured.

## V. Conclusion

Ferroelectric $HfO_2$, with a 10x improvement in coercive field over traditional materials and better process compatibility, is well positioned to make an impact in the memory market down the road. Using a TiN top electrode and a low temperature anneal of 600°C for 1hr, it may well be possible to fabricate ferroelectric $HfO_2$ devices using sputtered Al-doped $HfO_2$ films. Nevertheless, further research is required in order to verify this. The successful fabrication of MIM capacitors and testing on the TF 1000 would validate the presence of ferroelectricity in the samples. Alternatively, the effect of depletion capacitance on the hysteresis measurement could be ascertained and removed via post-processing, allowing analysis of MIS capacitors. If the solid source dopant samples are proven to be ferroelectric, the process can be further tuned and used to study the many potential applications of ferroelectric $HfO_2$ in semiconductor devices.

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